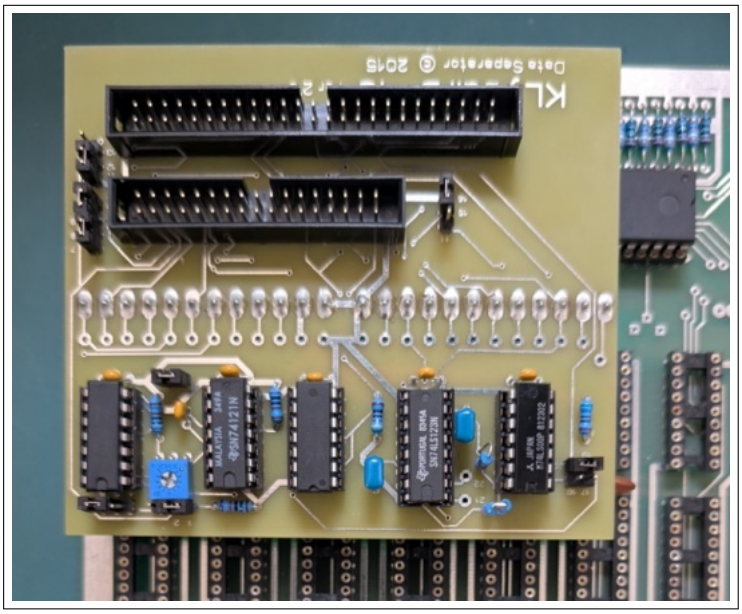

The KLyBall D13 Data Separator

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January, 2025

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1 Introduction

This document is a collection of notes relating to the build and installation of the KLyBall D13 Data Separator, based on information gained from members of the OSIWeb.org discussion forums (https://osiweb.org/osiforum/).

The notes and information here specifically apply to a D13 version 2 data separator used in conjunction with a OSI 600D coupled to a 610 expansion card.

Version 2 of the D13 data separator differs from version 1 in that it is ready for dual two sided drives *abcd* or any other combination, and has a motor control circuit if desired. Version 1 needed a modification for dual double sided drives. In addition there is a jumper to disengage the data separation and motor control.

2 Construction Notes

2.1 Components and Layout

The following is a 'bill of materials' (BOM) needed to populate the D13 data separator. The component layout is shown in **Fig. 2.1**.

```
C1   0.1 uF
C2   0.1 uF
C3   0.1 uF
C34  0.001 uF (1nF)
C35  0.1 uF
C36  0.1 uF
C39  100uf
C40  100uf

IC1  74LS06
IC4  74121 (not a 74LS121)
IC6  74ALS00
IC8  74LS123
U2B  7400 (a 74LS00 has proven to be fine)

R1   560R
R28  10K
R29  1K
R30  1K
R41  10K trimmer
R48  470R
R53  44k
R52  22k
```

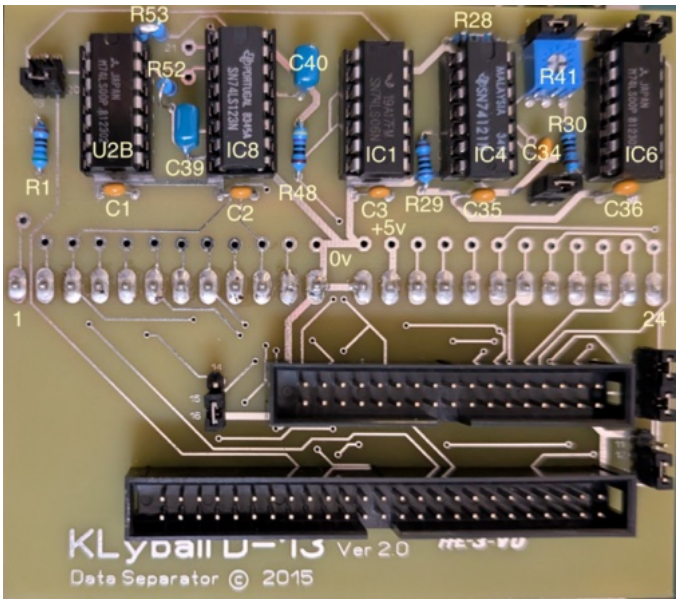

Figure 2.1: Component layout details.

2.2 Power Connection

Ensure that there is +5 supplied to pin 14 of the connector on the 610 expansion board. This may require a small jumper be added from +5V to this pin. See **Fig. 2.2** for details.

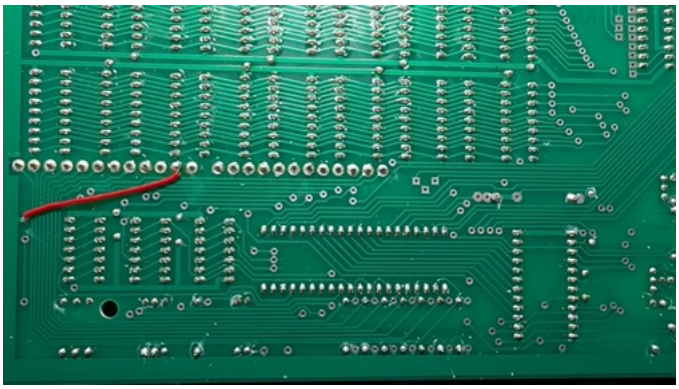

Figure 2.2: Adding a power connection.

3
Calibration and Configuration

3.1 OSI 610 Expansion Board

The transmit and receive clocks make use of four one-shot pulse generators, these can be calibrated by removing the D13 data separator and entering disk mode, by pressing *D* at the *D/C/W/M* prompt, and adjusting R18, R9, R10 and R19 as follows. See **Fig. 3.1** for details of the potentiometer locations.

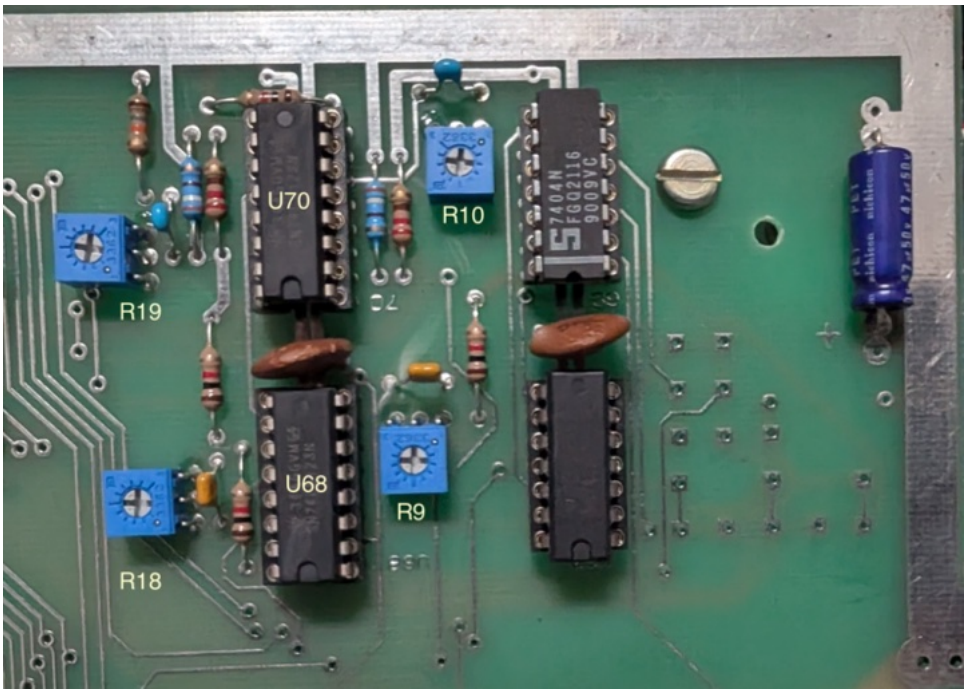

Figure 3.1: Location of potentiometers.

3.1.1 R18 TX CLOCK

Input of scope to pin 13 of U68. Adjust R18 for a positive pulse width of 400nSec +/- 50nS. See **Fig. 3.2**.

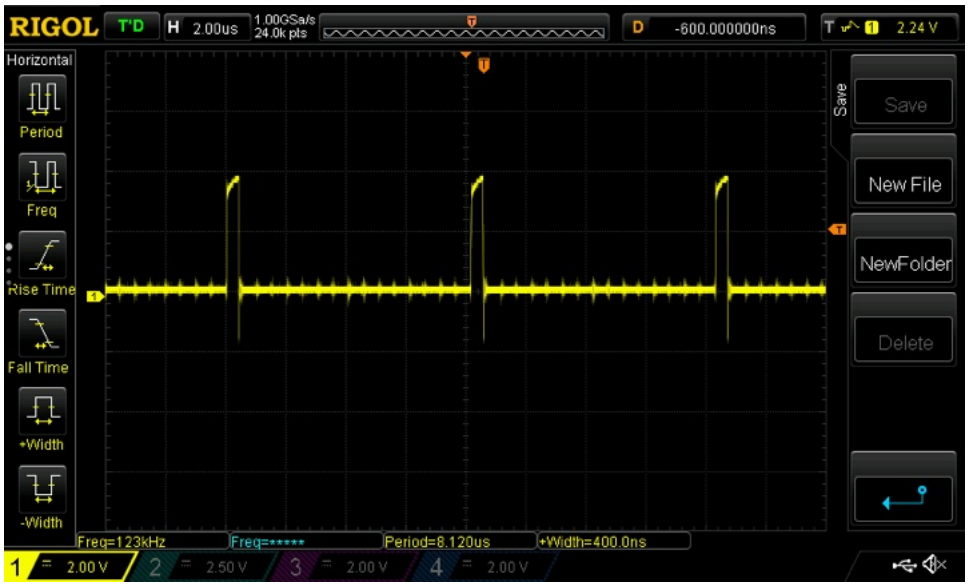

Figure 3.2: Adjusting R18.

3.1.2 R9 TX DATA

Input of scope to pin 12 of U68. Adjust R9 for a negative pulse width of 400nSec +/- 50nS. See **Fig. 3.3**.

3.1.3 R10 RX CLOCK

Connect a jumper from pin 9 of J3 to pin 10 of J3. Input of scope to pin 5 of U70, ee **Fig. 3.4**.. Adjust R10 for a positive pulse width of 1uS. See **Fig. 3.5**.

3.1.4 R19 RX DATA

Connect a jumper from pin 9 of J3 to pin 11 of J3. Input of scope to pin 4 of U70 see **Fig. ??**. Adjust R19 for a negative pulse width of 6uS. Remove

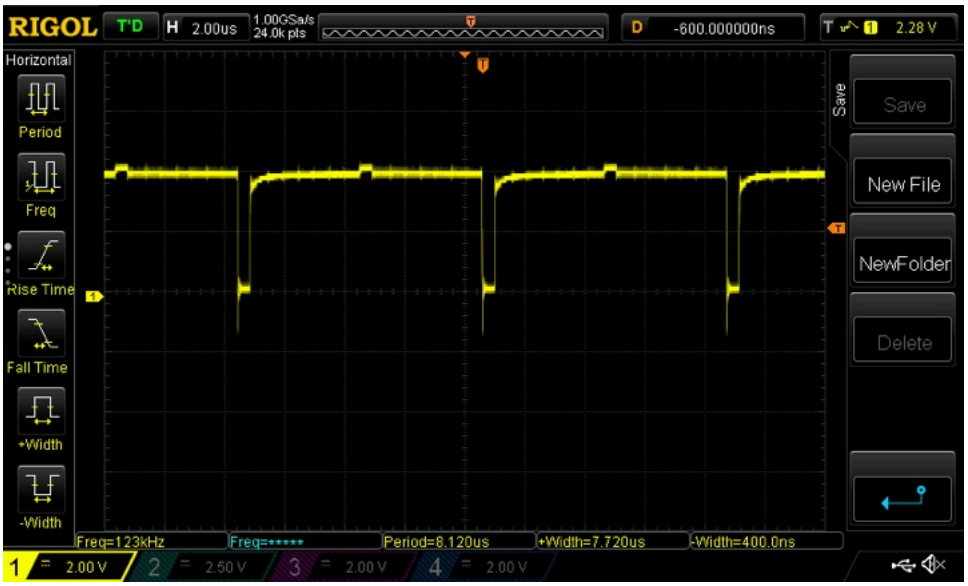

Figure 3.3: Adjusting R9.

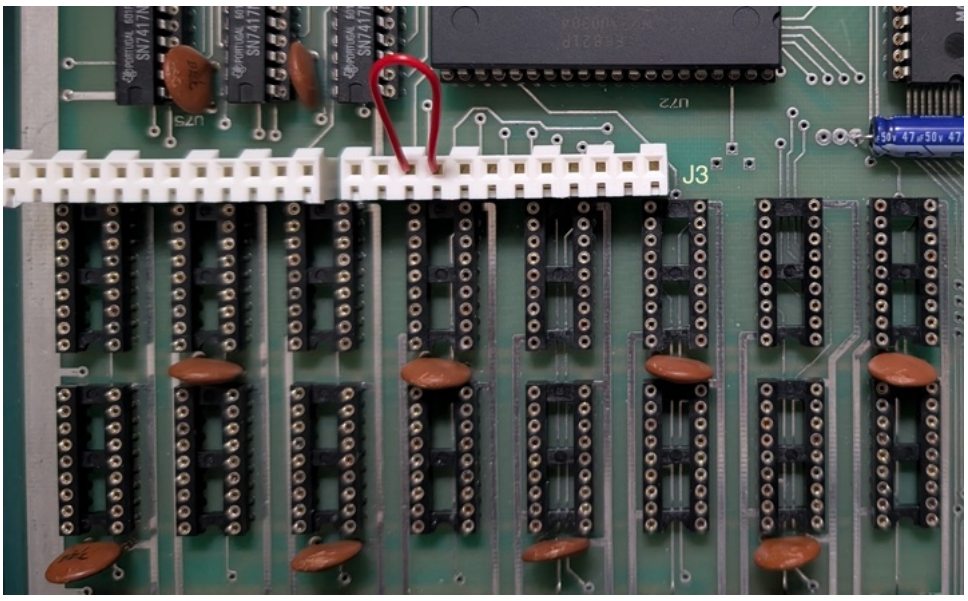

Figure 3.4: Jumper on J3, 9 to 10..

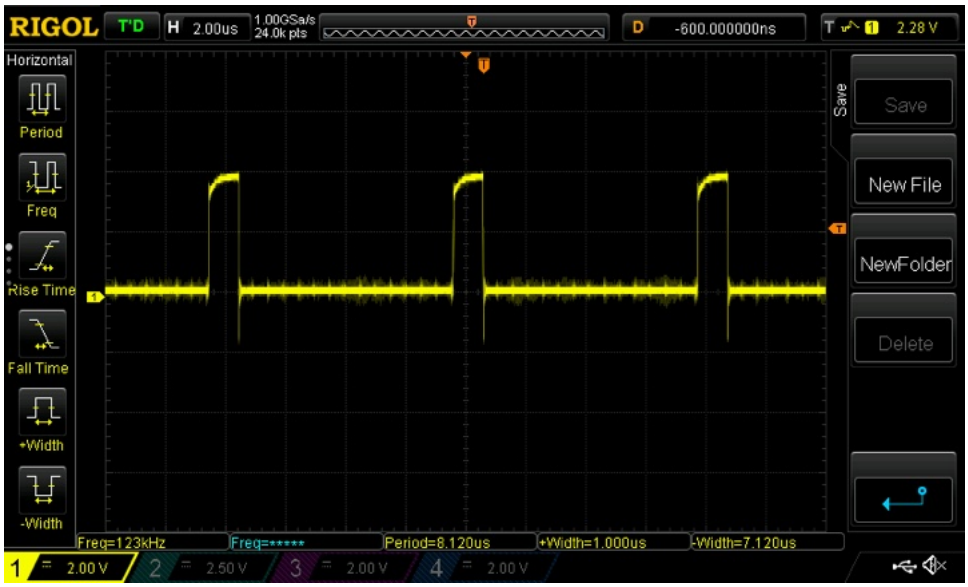

Figure 3.5: Adjusting R10.

jumper and reconnect J3. See **Fig. 3.7**.

Some experiment with R20 (18k) may be required to obtain the correct pulse width. A value of 10k may be more appropriate.

3.2 D13 Data Separator Board

With the board fitted, temporarily connect pin 9 of the 24 pin connector to link pin 1, see **Fig. 3.8**. With the system powered up and no drives connected, set the input of the scope to pin 1 of IC4 and adjust R41 for a negative width of 6us. See **Fig. 3.9**.

3.3 Link Settings

Please note that the links indicated on the schematic (see Appendices) are numbered differently to those on the board. Below is a table mapping the schematic diagram labels to the markings on the board itself.

```
Board Link      Schematic Link
```

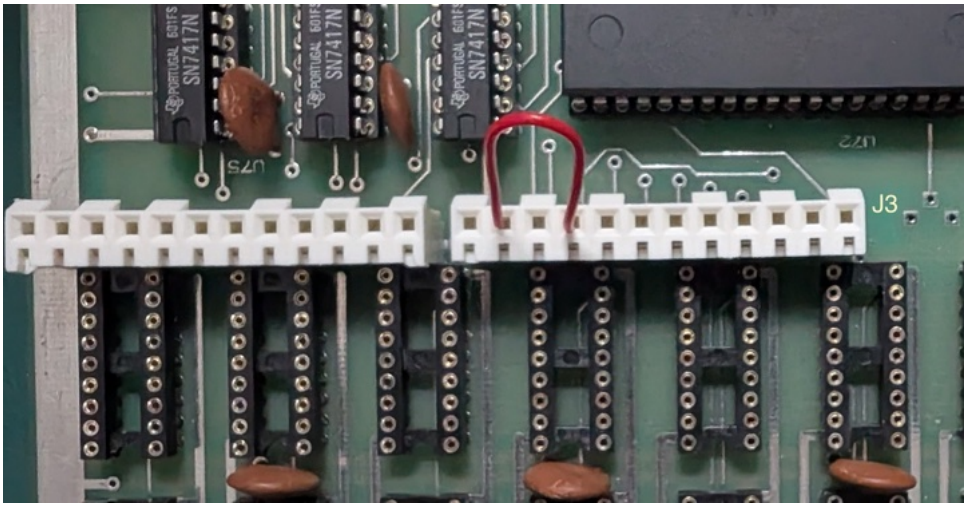

Figure 3.6: Jumper on J3, 9 to 11.

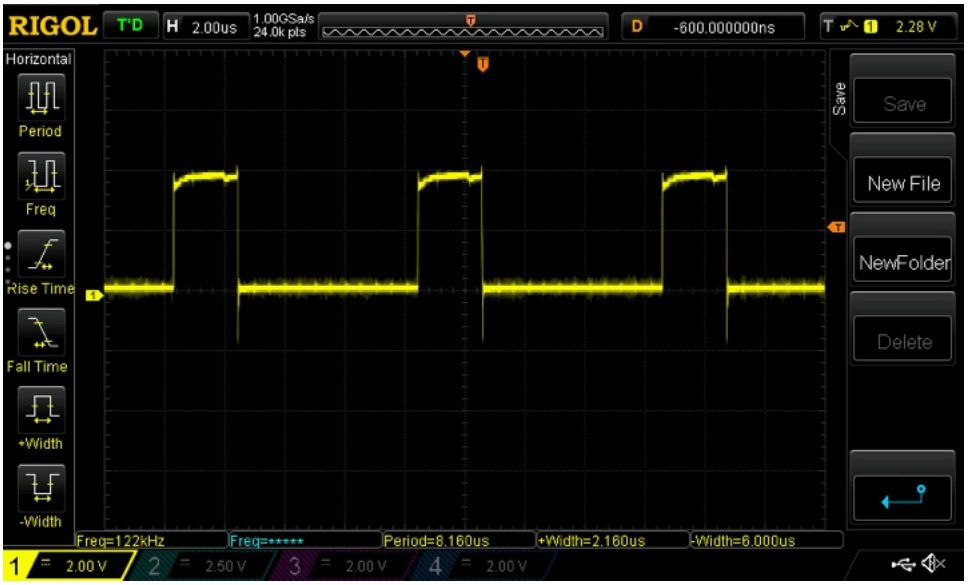

Figure 3.7: Adjusting R9.

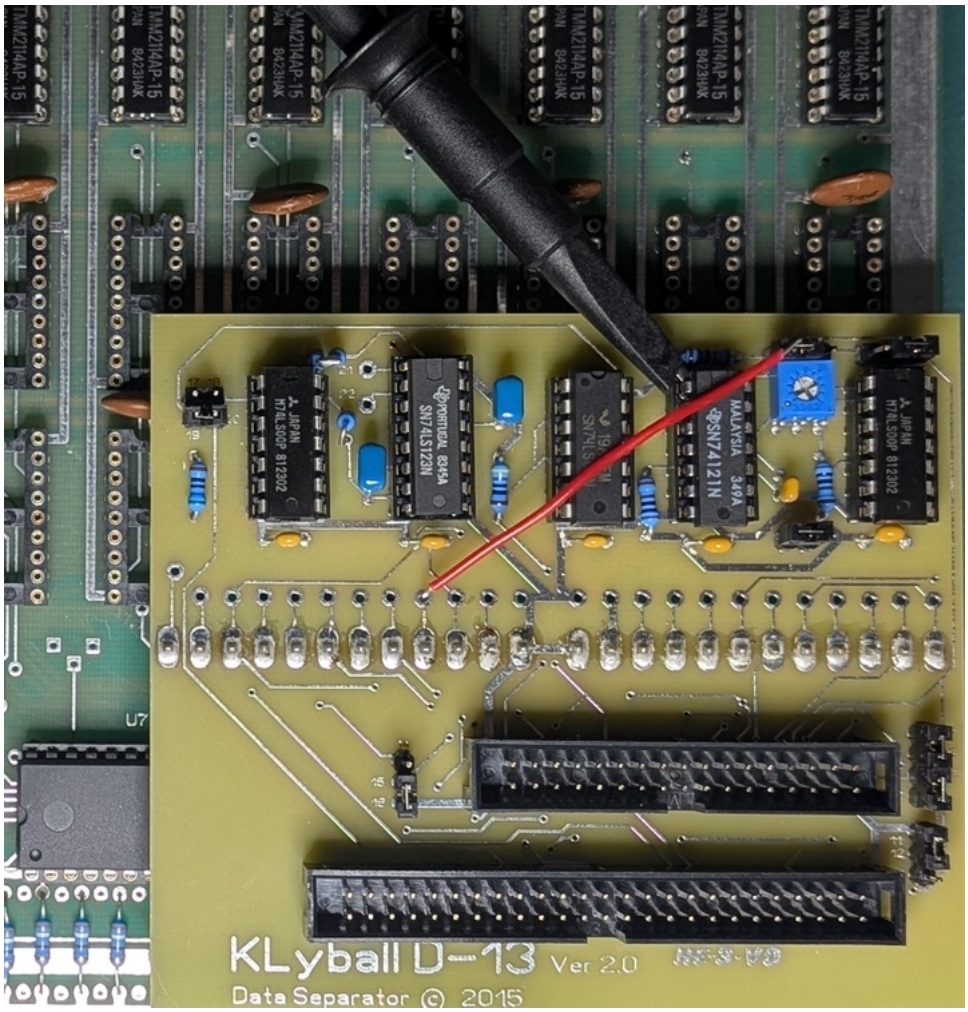

Figure 3.8: Temporary link.

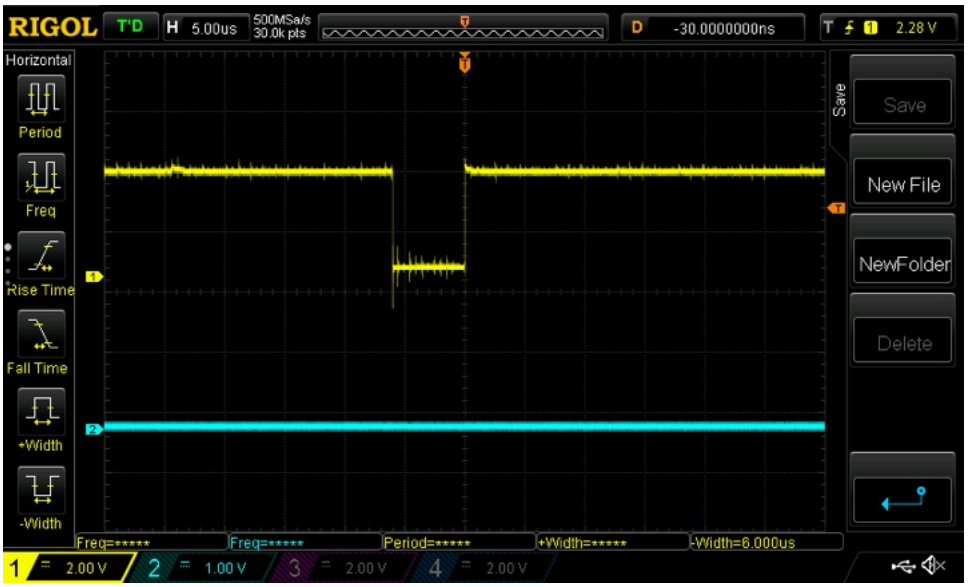

Figure 3.9: Adjusting R41.

Pin 1	JP30	Pin 3
Pin 2		Pin 2
Pin 3		Pin 1
Pin 4	JP33	Pin 1
Pin 5		Pin 2
Pin 6		Pin 3
Pin 7	JP35	Pin 4
Pin 8		Pin 3
Pin 9		Pin 2
Pin 10		Pin 1
Pin 11	JP 34	Pin 1
Pin 12		Pin 2
Pin 13		Pin 3
Pin 14	JP 1	Pin 3
Pin 15		Pin 2
Pin 16		Pin 1

Pin 17	JP 2	Pin 2
Pin 18		Pin 4
Pin 19		Pin 1
Pin 20		Pin 3

The following link (placed between IC4 and IC6) is not marked on the board.

a	JP 32	Pin 2
b		Pin 1

The following link settings have been shown to work with both a C1/SBII with 610 and a 5.25 inch drive, and a C2 with D&N board and a 5.25 inch drive.

Suggested links for 5.25 inch drives are shown below and in **Fig. 3.10**.

```
1-2
5-6
a-b (unmarked link placed between IC4 and IC6, see above)
7-8
9-10
11-12
15-16
19-20
```

3.4 Checking the board

With the Gotek attached, and a disk selected attach channel 1 of scope to the separated clock (pin 10 of the 24 way connector) and channel 2 to the separated data (pin 11 of the 24 way connector), and trigger the scope from channel 1. The data and clock signals should be clearly separated, see **Fig. 3.11**.

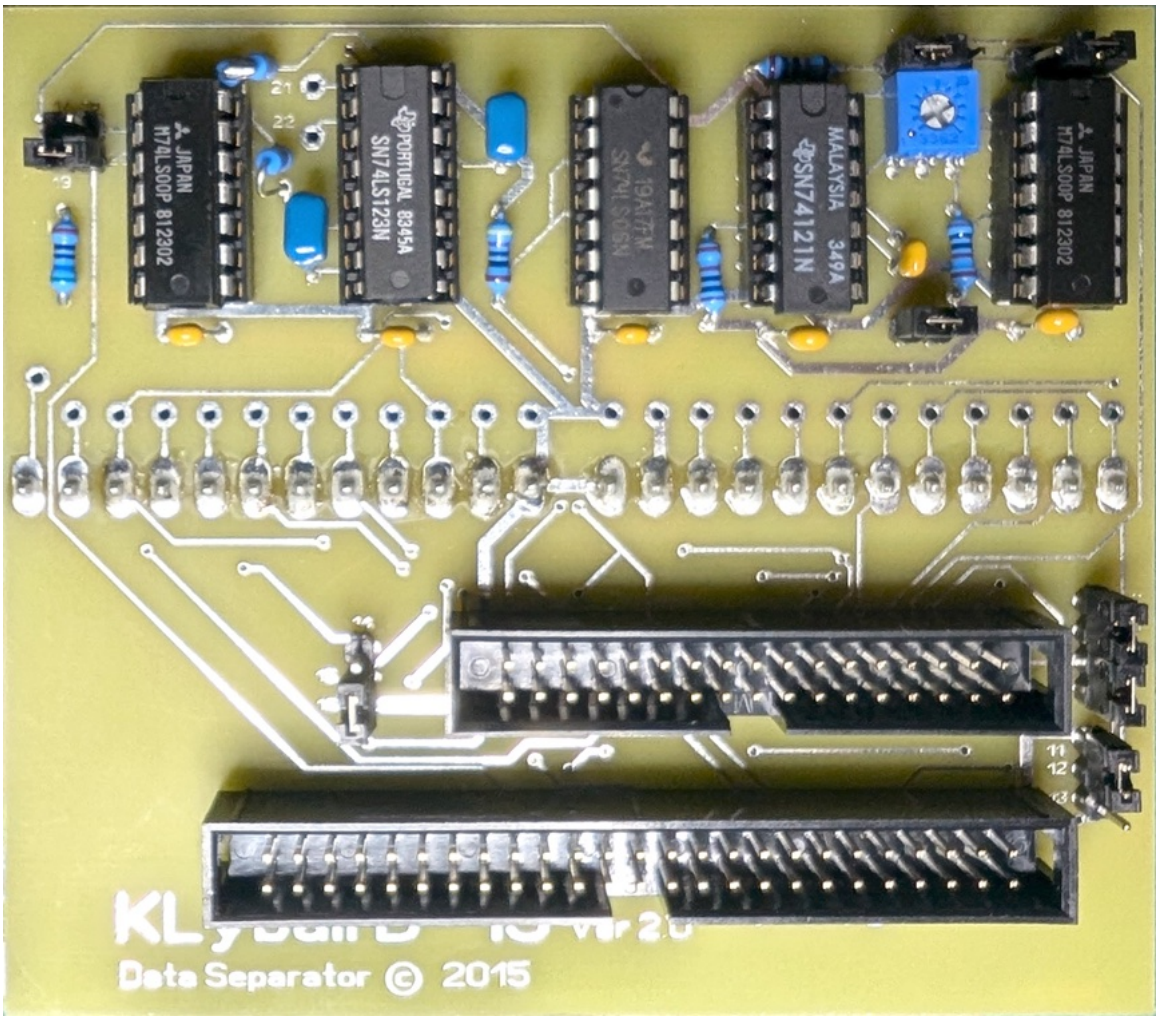

Figure 3.10: Link Settings.

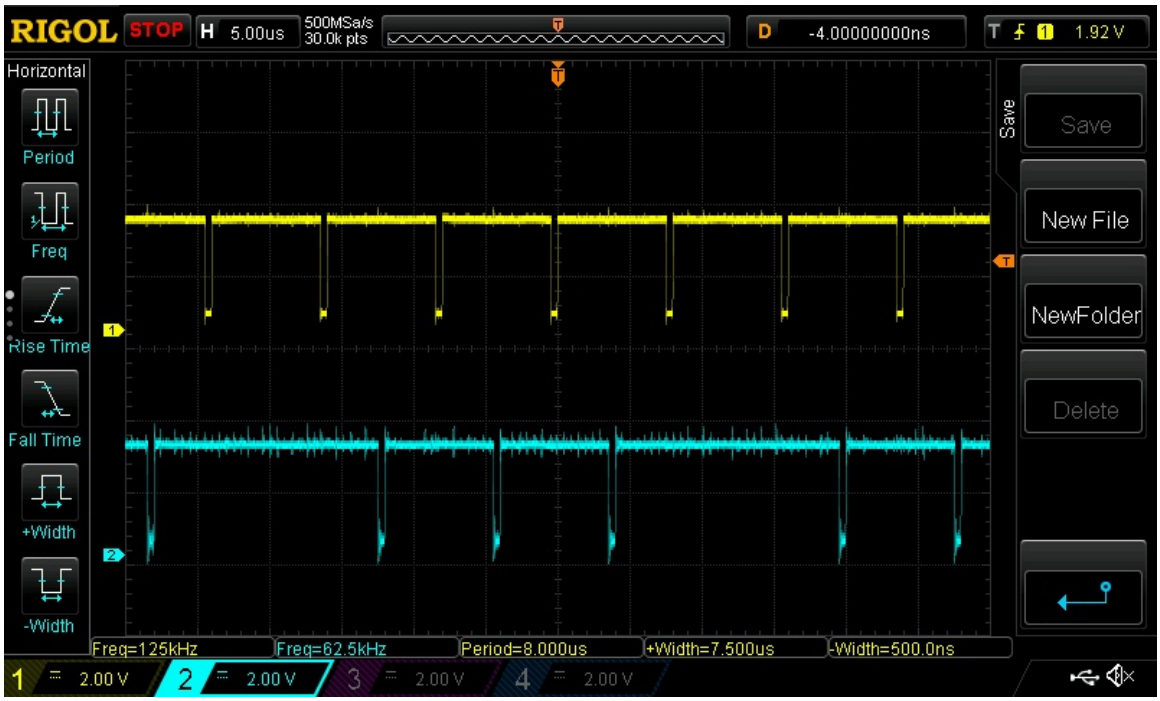

Figure 3.11: Separated signals. Clock shown yellow and data shown blue.

4 Disk Operation

4.1 Gotek Settings (FF.CFG)

The disk images tested with the Gotek were .hfe images created from published .65d disk images, with the OSIHFE (v1.4) utility.

To make an HFE file of Hexdos disk images for use with the Gotek drive, include the *-5* option on the OSIHFE command line.

These are the settings that have been found to work for a system configured for single sided drives. Some of these settings are the default settings, however, they are shown here for completeness.

```
interface = shugart
host = unspecified
pin02 = nc
pin34 = rdy
write-protect = no
max-cyl = 255
side-select-glitch-filter = 2
track-change = realtime
write-drain = instant
index-suppression = yes
head-settle-ms = 15 # also try 25 ms
motor-delay = 450
chgrst = step
```

Note that the *write-protect* setting within FF.CFG defaults to *no*. A setting of *no* means that Flash Floppy will respect the setting of the file's *Read Only* attribute and, therefore, may still be read only. A setting of *yes* will force readonly on start up but can be overridden by holding Gotek's eject button(s) for 2 seconds (see the Eject Menuhttps://github.com/keirf/flashfloppy/wiki/Initial-Setup#eject-menu) option in the FlashFloppy Wiki for more details.

4.2 Using Greaseweazle to Create Physical Disks

The ȯ65d images are typically single sided, single density disks designed for 48tpi drives. When converting them to .hfe disk images (see above) they need to be represented as double sided disks with the .65d image on side 0 of the .hfe disk image.

Using a 48tpi disk drive such as a Teac 55B set to DS0 with a straight cable, the following command can be used. Note that the disk is written as a low density (*–densel L*) single sided disk. Note that some versions of Greaseweazle do not use the longform versions for low density (*–densel L*), in this case, use the *-dd* option instead.

```
gw write --drive=0 --erase-empty --densel L
    --tracks="c=0-39:h=0:step=1" mydisk.hfe
```

4.3 Testing the 610 ACIA

This program will actually generate a square wave from the ACIA on the 610 board. Enter it using the Monitor and execute from $4000:

```
4000  A9 03     LDA #3
4002  8D 10 C0  STA $C010
4005  A9 15     LDA #$15
4007  8D 10 C0  STA $C010
400A  A2 55     LDX #$55
400C  AD 10 C0  LDA $C010
400F  29 02     AND #2
4011  F0 F9     BEQ $400C
4013  8E 11 C0  STX $C011
4016  D0 F4     BNE $400C
```

4.4 Testing Track Zero Loading

You can check if track 0 is in fact loading by going into the Monitor and entering .FC06G. That should cause track 0 to be loaded, and the CPU then return to the Monitor program. The first five bytes at $2200, with either 65D or Pico-Dos, should be;

```
A9 01 8D 5E 26.
```

4.5 Testing the Floppy Disk System

David Gesswein has created a floppy test program for 5.25 and 8 inch disks full details can be found at https://www.pdp8online.com/osi/osi-floppy-test.shtml.

The program auto configures for serial and video systems. It can be used via serial on video based systems such as C1PMF that has a smaller display, which allows you to see complete diagnostic information. It can check RPM speed, disk interface signals, Read and Write ability and more.

If the system, does not boot but passes the disk tests within the above mentioned floppy disk test program. It may be worth re-calibrating the D13 board by starting with the trimmer set a minimum value and repeatedly trying to boot the disk e.g. 'Break' followed by 'D' with slowly increasing values. If it boots, keep increasing the value until it no longer boots, then set the trimmer to halfway between the two positions.

4.6 Memory Test

Be aware that any RAM "issues" above 8k will prevent a disk from booting. No error is reported, just boot failure!

A memory test can be performed using the following BASIC program.

For example, to test a 610 board populated with 24K of RAM, enter a. start page of 32 and an end page of 95. This will test memory from 8192h to 5FFFh.

```
650 REM MEMORY TEST BY W.L. TAYLOR
660 PRINT " ******MEMORY TEST****** ":PRINT
665 PRINT " ENTER STARTING AND ENDING PAGE":PRINT
700 INPUT "STARTING PAGE ";P1
710 INPUT "ENDING PAGE ";P2
720 D=0
730 LET A=P1*256
740 LET B=P2*256
750 FOR C=A TO B
```

```
760 POKE C,D
770 E=PEEK (C)
780 IF E<>D THEN PRINT " BAD DATA BYTE AT";C
790 IF E<>D THEN END
800 NEXT C
810 D=D+1
820 IF D<256 THEN 750
830 IF D=256 THEN PRINT " NO BAD DATA DETECTED":PRINT
840 END
```

4
Appendix A - Schematics

Pin assignment for the D13 24 pin connector, referred to as J3 on the 610 expansion board.

Pin 24 is nearest the edge of the 610 circuit board.

```
 1  Head Load
 2  Low Current
 3  Drive Select 1 & 2
 4  Fault Reset
 5  Step
 6  Direction
 7  Erase Enable
 8  Write Gate
 9  Write Data
10  Separate Clock
11  Separate Data
12  Ground
13  Ground
14  +5V (not connected)
15  -9V (not used)
16  N.C.
17  Index
18  Side Select
19  Write Protect
20  Ready Drive 2
21  Sector (not used)
22  Fault (not used)
23  Track 00
24  Ready Drive 1
```

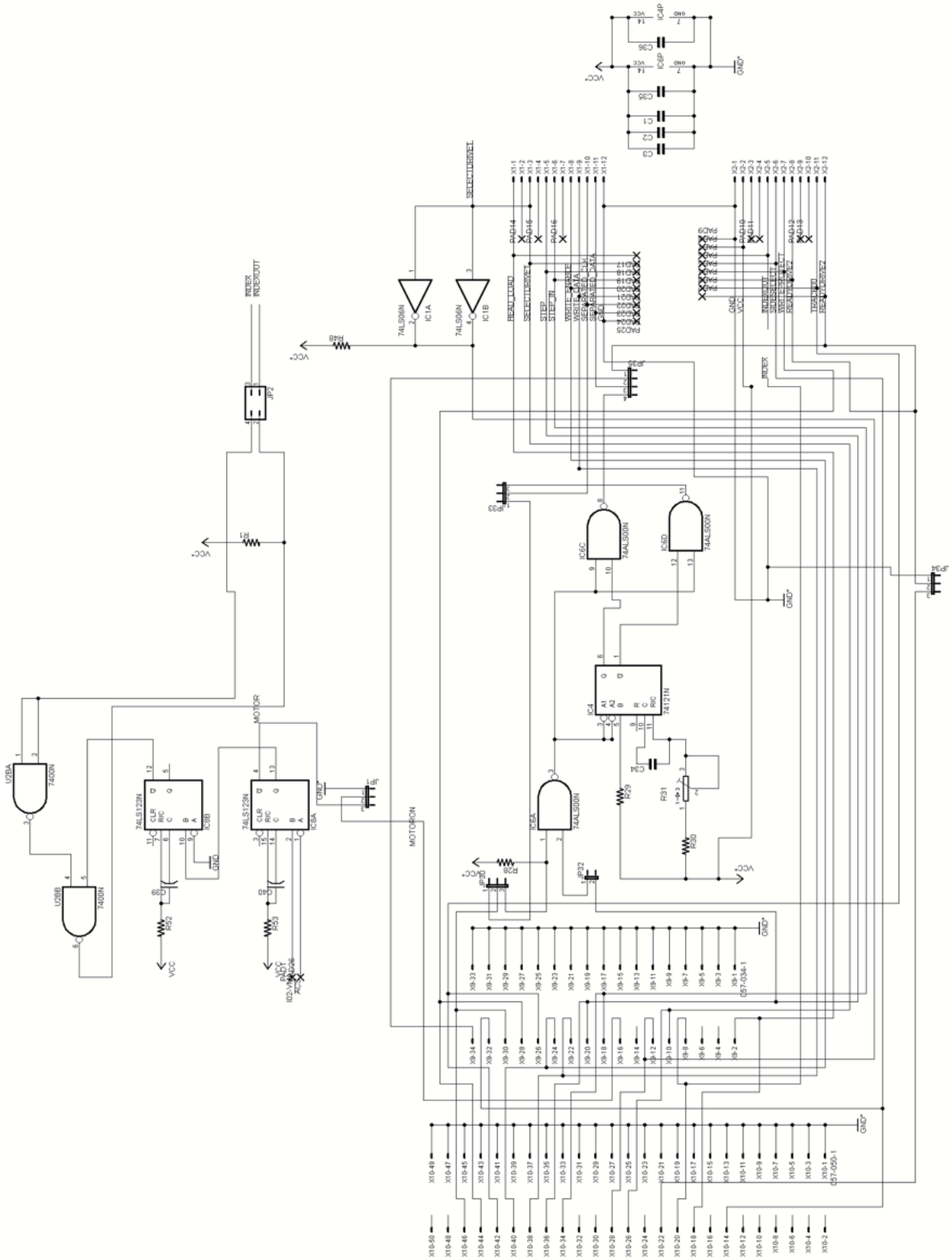

Figure 4.1: Schematic Diagram.

Notes: